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(54) Microwave monolithic integrated circuit testing.

(57) RF performance measurements are performed on basic transistors (11) of a microwave monolithic integrated circuit while it is being fabricated. The circuitry necessary to assess the performance potential at the frequency and power levels of interest is provided by incorporating matching elements (23, 24) onto RF probes (12, 13) used for in-process tests. The RF performance potential of monolithic integrated circuits is being measured at an early stage in the process before expensive process sequence has been completed. The transistors are measured with an RF probe (12, 13) that has RF matching circuitry (23, 24) included as an integral part of the probe (12, 13). Consequently, the performance potential of circuits on the wafer is assessed at the earliest possible point in the manufacturing process.

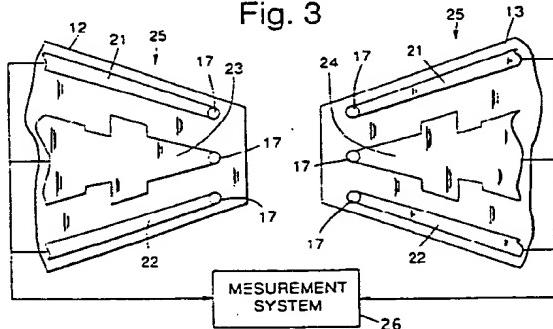


Fig. 3

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BACKGROUND

The present invention relates generally to microwave monolithic integrated circuits, and more particularly, to a microwave monolithic integrated circuit fabrication and test method and test circuits that determine the performance potential of the circuits during the manufacturing process.

Currently, the cost to produce a GaAs microwave monolithic integrated circuits is \$5,000 to \$10,000 per wafer. However, not all completed circuits produce acceptable RF performance. Transistors are RF testable as soon as the basic transistor structure is completed, which is 30-40% of the way through the manufacturing process. Currently RF tests are performed on completed wafers. The conventional method for testing completed wafers is to evaluate completed microwave monolithic integrated circuits using on-wafer RF probes coupled to a 50 ohm measurement system.

Two methods are commonly used to assess performance potential of microwave monolithic integrated circuit wafers. DC tests can be performed early in the process sequence (at the same point as the present invention implements RF tests). However, the correlation between the DC tests and RF results is not good. Therefore, the risk of rejecting "RF good wafers" or processing "RF bad" wafers based solely on DC test results is high. An alternative is to perform tests after completion of wafer processing. The problem with this approach is that significant value has been added to wafers that could have been tested earlier and found to be "RF bad". Any funds expended on wafers known (or even unknown) to be "RF bad" are wasted since the wafer costs are unrecoverable after processing is completed.

The current approaches to assessing performance potential early in the process sequence have been to take DC measurements of transistor current-voltage characteristics. Unfortunately, the correlation between these measurements and the RF performance of the completed circuits is relatively poor at this stage of the technology evolution. An alternative technique which has been proposed is to measure the circuit performance at some frequency well below its intended operating frequency; for example, 2 GHz for a circuit intended for 10 GHz operation. Again, the correlation between low frequency test results and higher frequency performance is not as good as desired.

Therefore, it is desirable to measure the performance potential of a wafer as soon as possible in the process so that "RF bad" wafers are not processed to completion. A significant savings would result if the performance potential of microwave monolithic integrated circuits could be assessed early in the manufacturing process.

SUMMARY OF THE INVENTION

In order to eliminate the waste inherent in processing microwave monolithic integrated circuits to completion and then testing them for RF capabilities, in the present invention, the RF performance measurements are performed on the basic transistors which comprise the microwave monolithic integrated circuits. The circuitry necessary to assess the performance potential at the frequency and power levels of interest is provided by incorporating matching elements onto the on-wafer RF probes used for in-process tests.

The present invention measures the RF performance potential of GaAs monolithic microwave integrated circuits at an early stage in the process before the expensive process sequence has been completed. The essence of the invention is that the transistors formed at wafer test sites are measured with an RF probe having RF matching circuitry included as an integral part of the probe. Consequently, the performance potential of circuits on the wafer is assessed at the earliest possible point in the manufacturing process; specifically at the time Schottky barrier gates, for example, are deposited.

This in-process measurement approach may be applied to any microwave monolithic integrated circuit. Once the correlation between in-process and post-process measurement results are established, the present method may be used to routinely screen wafers, thereby saving roughly two-thirds of the processing cost of "RF bad" wafers.

Thus, to summarize the present invention, it is a GaAs microwave monolithic integrated circuit fabrication and test method comprising the following steps. Fabricating a plurality of GaAs microwave monolithic integrated circuits, including a plurality of test transistors, such that active layers, interconnect layers, contacts, and gates are formed, which integrated circuits and test transistors comprise operational transistors. Performing DC and RF testing of the test transistors to determine operability of the operational transistors. If the test transistors are operable and perform in a proper manner, then completing fabrication of the plurality of GaAs microwave monolithic integrated circuits.

BRIEF DESCRIPTION OF THE DRAWINGS

The various features and advantages of the present invention may be more readily understood with reference to the following detailed description taken in conjunction with the accompanying drawings, wherein like reference numerals designate like structural elements, and in which:

Fig. 1 illustrates a typical GaAs wafer incorporating monolithic microwave integrated circuits and

test site location containing transistors for RF on-wafer probing in accordance with the principles of the present invention;

Fig. 2 shows a coplanar transistor and probes designed for probe-matched, on-wafer testing in accordance with the principles of the present invention;

Fig. 3 shows RF probes with impedance matching circuitry appropriate for probe-matched, on-wafer testing in accordance with the principles of the present invention; and

Fig. 4 shows a typical GaAs microwave monolithic integrated circuits process sequence in accordance with the principles of the present invention.

DETAILED DESCRIPTION

Referring to the drawing figures, Fig. 1 illustrates a typical GaAs wafer 10 incorporating monolithic microwave integrated circuits 20a, and test site locations 20b containing transistors 11 for RF on-wafer probing in accordance with the principles of the present invention. More particularly, the wafer 10 is shown having two types of integrated circuit areas. The blank areas represent monolithic microwave integrated circuits 20a. The shaded areas represent process control monitor sites, comprising the test site locations 20b, that include as one element among many, a coplanar transistor 11, for example, as is shown in Fig. 2.

Fig. 2 shows the coplanar transistor 11 which is part of a GaAs microwave monolithic integrated circuit test pattern located at the test site locations or reticles 20b, and which is repeated periodically across a GaAs monolithic integrated circuit wafer 10. Probes 12, 13 are shown disposed above the wafer 10 that are designed for on-wafer testing in accordance with the principles of the present invention. Fig. 2 shows a top view of the test site location 20b looking at the top surface of the transistor 11, and wherein the probes 12, 13 overlay the surface of the transistor 11. Probe contact pads 17 are disposed in contact with the corresponding pad areas of the transistor 11 during the DC and RF measurement sequence. Fig. 3 shows the details of the RF probes 12, 13 showing impedance matching circuitry 23, 24 appropriate for probe-matched, on-wafer testing in accordance with the principles of the present invention. More particularly, Fig. 3 shows an underside view of the probes 12, 13 illustrating the details of the impedance matching circuitry 23, 24.

More particularly, and with reference to Fig. 2, the coplanar transistor 11 is typically a Schottky barrier field effect transistor 11, for example, that is comprised of a source 14, a drain 15, and a gate 16. Overlaying the transistor 11 are the two RF

probes 12, 13 that each have three probe contacts 17. The probe contacts 17 are shown in phantom since they are on the bottom surface of the probes 12, 13. Each of the three probe contacts are sized and spaced so that they contact the source 14, drain 15 and gate 16. With reference to Fig. 3, the outermost probe contacts 17 of each RF probe 12, 13 provide RF and DC ground connections by way of two conductors 21, 22, while the respective central probe contacts 17 provide RF signal and DC bias connections through input and output impedance matching circuitry 23, 24 that is disposed on the underside of the probes 12, 13.

The coplanar transistor 11 of Fig. 2 is designed for probe-matched on-wafer testing in accordance with the principles of the present invention. This transistor 11 is RF performance evaluated after Schottky gate or first interconnect metal deposition, as will be described below with reference to Fig. 4. This testing is performed much earlier in the manufacturing process than is conventionally possible, thereby saving the cost of processing wafers 10 that do not meet RF performance standards.

The RF probes 12, 13 shown in Fig. 3 incorporate input and output impedance matching circuitry 23, 24 that is appropriate for probe-matched, on-wafer testing in accordance with the principles of the present invention. RF probes 12, 13, such as those manufactured by Cascade Microtech, of Beaverton, Oregon, for example, have been adapted to include impedance matching circuitry 23, 24 appropriate for the frequency band and signal level of interest, and are imprinted using a coplanar transmission line impedance matching probe structure 25. The impedance matching probe structure 25 forms a microwave transition between the planar transistor 11 and a 50 ohm measurement system 26 that typically employs coaxial microwave terminals.

The term GaAs microwave monolithic integrated circuit 20a as used herein is any circuit, whether it is manufactured in silicon or gallium arsenide or related compound semiconductor material, that performs what is normally considered to be a microwave function. Likewise, the term Schottky barrier field effect transistor 11 used to describe the microwave function evaluated according to the principles of the present invention may be any type of passive or active microwave function including field effect transistors, bipolar transistors, metal oxide field effect transistors or two terminal microwave devices such as PIN diodes, IMPATT diodes or Gunn diodes, for example. Furthermore, the coplanar transmission line structures referred to herein represent any type of RF transmission lines including coplanar and microstrip transmission lines, and the like, for example.

Fig. 4 shows a representative process sequence 30 or method 30 in accordance with the principles of the present invention that is adapted for use in testing the GaAs microwave monolithic integrated circuit wafer 10. The method 30 shown in Fig. 4 also identifies test points at which time the integrated circuit wafer 10 is tested. Such a GaAs microwave monolithic integrated circuit wafer 10 is tested with the transistors 11 and impedance matching probes 12, 13 shown and described with reference to Figs. 2 and 3. Typical impedance matching probes 12, 13 that may be adapted for use in the present method 30 are manufactured by Cascade Microtech of Beaverton, Oregon.

The Cascade Microtech probes 12, 13 cited herein are typical of those used to interface measurement systems with RF monolithic microwave circuits in wafer form. However, other probes, such as membrane probes that serve the same purpose and may be adapted to implement the same impedance matching functions described above, and may be employed in accordance with the teachings of the present invention. Accordingly, such membrane probes are represented by the Cascade probes described herein.

GaAs microwave monolithic integrated circuit production yield is conventionally quite low due to the immaturity of the fabrication process. In the production process, the transistors 11 that form the active devices in the GaAs microwave monolithic integrated circuit 20a are completed relatively early in the production sequence, at about 30-40% of the way through the overall process sequence. However, RF matching circuitry necessary to test these circuits 20a as multi-stage amplifiers is not completed until the last step of the production sequence. Consequently, significant savings in development and production costs is achieved in accordance with the method 30 of the present invention by determining the performance potential of the circuits 20a early in the process sequence.

The present invention circumvents most of the problems prevalent in the art by testing the performance of the individual transistors 11 of the circuits 20a as soon as they are fabricated. The circuits 20a are testable as functional transistors as soon as the Schottky barrier gates 16 have been deposited. The present invention thus provides a means for testing the circuits 20a at the earliest possible point in the manufacturing process.

With reference to Fig. 4, it shows the GaAs microwave monolithic integrated circuit process sequence 30 in accordance with the principles of the present invention. This process sequence 30 is one of many that may be employed, and of which the present invention may be incorporated to provide for integrated circuit testing. Also included in Fig. 4 are references to typical test points during the

process sequence 30. Clearly it is advantageous to test at the point in the process sequence 30 provided for by the present invention rather than at the very end as is conventionally done. A slight modification to the normal manufacturing process is required and is described below.

The method 30 is as follows. The first step 31 forms active layers on a substrate, by means of ion implantation, for example. The next step 32 isolates active devices (transistors 11) by implantation or mesa etching, for example. Then, ohmic contacts are deposited in step 33. Then, Schottky gates are deposited in step 34, and the transistors 11 are operational. A first level interconnect is then deposited in step 35. Preliminary DC and RF screening in accordance with the present invention is then performed to determine transistor performance in step 36. Dielectric isolation and via etching is then performed in step 37.

Then, second level interconnects are deposited in step 41. Air bridges are then formed in step 42. At this point, front side wafer processing is completed and front side DC testing is performed, also indicated in step 42. Wafer thinning is then performed in step 43. A back side via etch is then performed in step 44. Back side metalization is then deposited in step 45 and back side processing is complete. Functional circuit DC and RF testing is then performed, also indicated in step 45.

In accordance with the present invention, either at the point of ohmic contact or gate level metal deposition, steps 33 or 34, additional pads are added to provide coplanar line transition to the on-wafer probes 12, 13, as is indicated in step 51. Thus, individual transistors 11 that are representative of the performance of the transistors on the wafer 10 are available for RF probing. The transistors 11 are available from the test reticles 20b formed on the wafer 10. The individual transistors 11 are tested at specific frequencies in a specific mode of operation; for example, low noise or large signal, high power. The means for testing in specific modes is provided by the on-wafer matching circuitry 23, 24, which are provided on the probes 12, 13.

Referring again to Fig. 2, the transistor 11 to be tested is shown, while the probes 17 with deposited matching circuitry 23, 24 are shown in Fig. 3. The matching circuitry 23, 24 provides an RF signal environment very near to that which would be obtained with on-wafer printed matching circuitry fabricated in conventional practice. Since the RF environment is much like the actual operating conditions expected from the circuit 20a in its final configuration, the early tests of the transistors 11 achieve by the present invention provide an excellent indication of the performance potential of the devices employed in the microwave monolithic

integrated circuit 20a. The matching circuitry 23, 24 provides appropriate impedance levels at appropriate frequency bands and is printed onto the coplanar RF test probes 12, 13. These probes 12, 13 provide the impedance transformation between the conventional 50 ohm measurement system 26 and the transistors 11.

To summarize the probe-matched, on-wafer testing of the present invention, the integrated circuit wafer 10 is processed in a normal manner to fabricate monolithic integrated circuits 20a, 20b thereon. After either gate or first interconnect metal deposition, the transistors 11 disposed at the test site locations 20b are evaluated for RF performance. This is accomplished by placing the probes 12, 13 onto the surface of the transistors 11 and testing the transistors 11 in a conventional manner. If the transistors 11 perform as desired, then the wafer fabrication process is continued and the wafer 10 is processed to completion.

The testing of the transistors 11 on the wafer 10 using the pre-matched probes 17 provides an excellent indication of whether the transistors 11 on the wafer 10 will function as expected. This is an extremely cost-effective method 30 of early evaluation of GaAs microwave monolithic integrated circuits 20a.

Thus there has been described a new and improved microwave monolithic integrated circuit fabrication and test method and test circuits that determine the performance potential of the circuits during the circuit manufacturing process. It is to be understood that the above-described embodiment is merely illustrative of some of the many specific embodiments which represent applications of the principles of the present invention. Clearly, numerous and other arrangements can be readily devised by those skilled in the art without departing from the scope of the invention.

Claims

1. A monolithic integrated circuit fabrication and test method comprising the steps of:
fabricating a plurality of monolithic integrated circuits (20a, 20b) including a plurality of test transistors (11), such that active layers, interconnect layers, contacts, and gates are formed, which integrated circuits (20a, 20b) and test transistors (11) comprise operational transistors;
performing DC and RF testing of the test transistors (11) to determine operability of the operational transistors;
if the test transistors (11) are operable and perform in a predetermined manner, then completing fabrication of the plurality of monolithic integrated circuits (20a).
2. The method of Claim 1 wherein the step of performing DC and RF testing comprises the steps of:
depositing interconnection pads (17) on the surface of the test transistors (11) to provide for coplanar line transitions to probes (12, 13) that are subsequently disposed thereon to performing DC and RF testing.
3. The method of Claim 2 which further comprises providing matching circuitry (23, 24) having desired impedance levels at predetermined frequency bands that is coupled to the interconnection pads (17) and which provide an impedance transformation between a measurement system (26) and the microwave monolithic integrated circuit (20a).
4. The method of Claim 3 wherein the matching circuitry (23, 24) is incorporating in or printed onto coplanar RF test probes (12, 13).
5. The method of Claim 3 or Claim 4 wherein the measurement system (26) is a 50 ohm measurement system (21).
6. The method of any of Claims 1 - 5 wherein the step of fabricating a plurality of monolithic integrated circuits (20a) including a plurality of test transistors (11) comprises the step of fabricating a plurality of field effect transistors and/or a plurality of metal oxide field effect transistors and/or a plurality of bipolar transistors.
7. The method of any of Claims 1 - 6 wherein the step of fabricating a plurality of monolithic integrated circuits (20a) including a plurality of test transistors (11) comprises the step of fabricating a plurality of two terminal microwave devices.
8. The method of Claim 7 wherein the step of fabricating a plurality of two terminal microwave devices comprises the step of fabricating a plurality of PIN diodes and/or a plurality of IMPATT diodes and/or a plurality of Gunn diodes.
9. The method of any of Claims 3 - 8 wherein the step of providing matching circuitry (23, 24) having desired impedance levels at predetermined frequency bands comprises the step of providing a coplanar transmission line structure and/or microstrip transmission lines.
10. The method of any of Claims 1 - 9 wherein said monolithic integrated circuits (20a) are

fabricated as GaAs microwave monolithic integrated circuits.

11. Test probes (12, 13) for testing a monolithic integrated circuit (20a) comprising:
- first and second substrate (12, 13);
 - three probe contacts (17) disposed on each respective substrate (12, 13), and wherein each of the three probe contacts (17) are sized and spaced to contact a source (14), drain (15) and gate (16) of a transistor (11) of the monolithic integrated circuit (20a);
 - input and output matching circuitry (23, 24) respectively disposed on the first and second substrates (12, 13) and coupled to respective center probe contacts (17);
 - first and second conductors (21, 22) respectively coupled to the outermost probe contacts (17);
 - and wherein the outermost probe contacts (17) provide RF and DC ground connections to a DC and RF measurement system (26) by way of the two conductors (21, 22), and wherein the respective central probe contacts (17) provide RF signal and DC bias connections to the DC and RF measurement system (26) through the input and output matching circuitry (23, 24).

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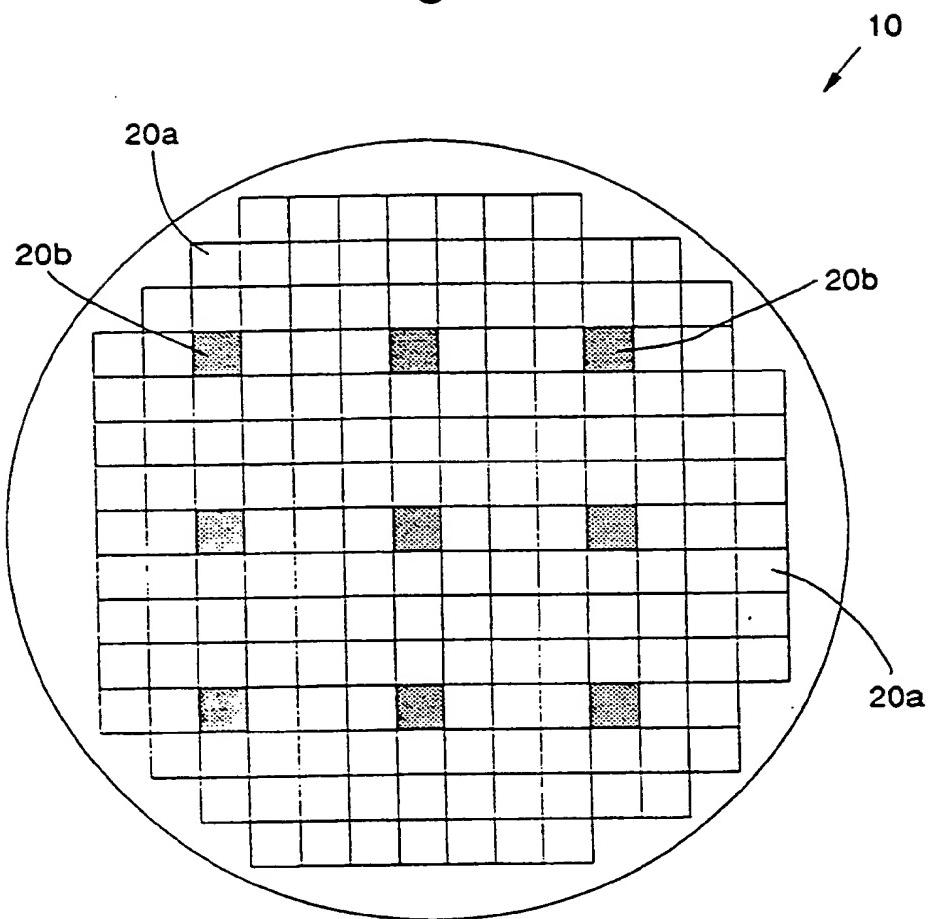
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Fig. 1



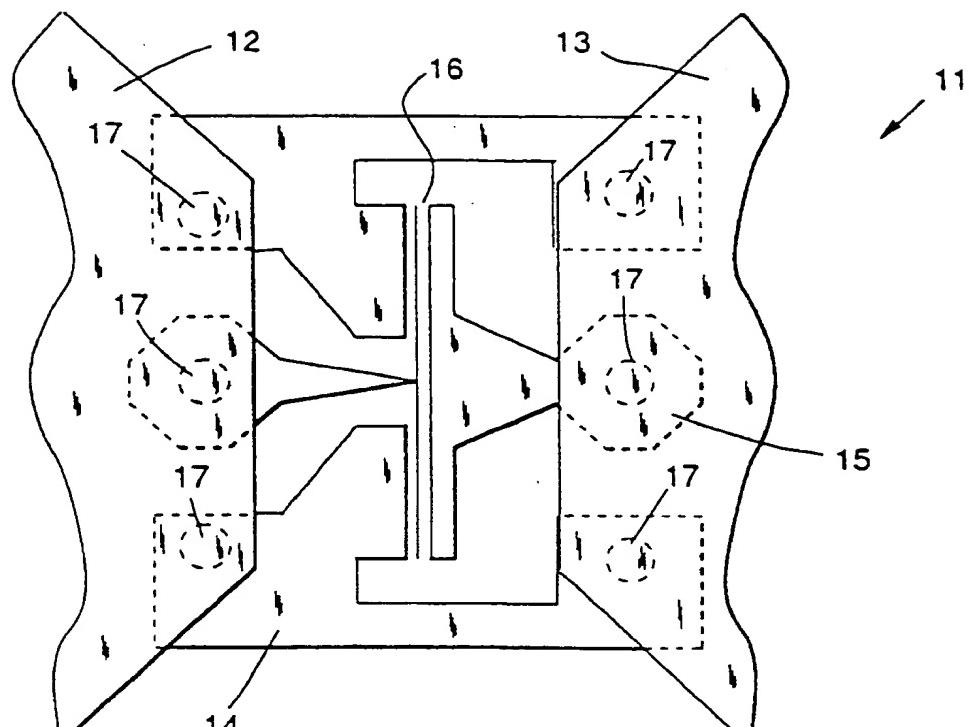


Fig. 2

Fig. 3

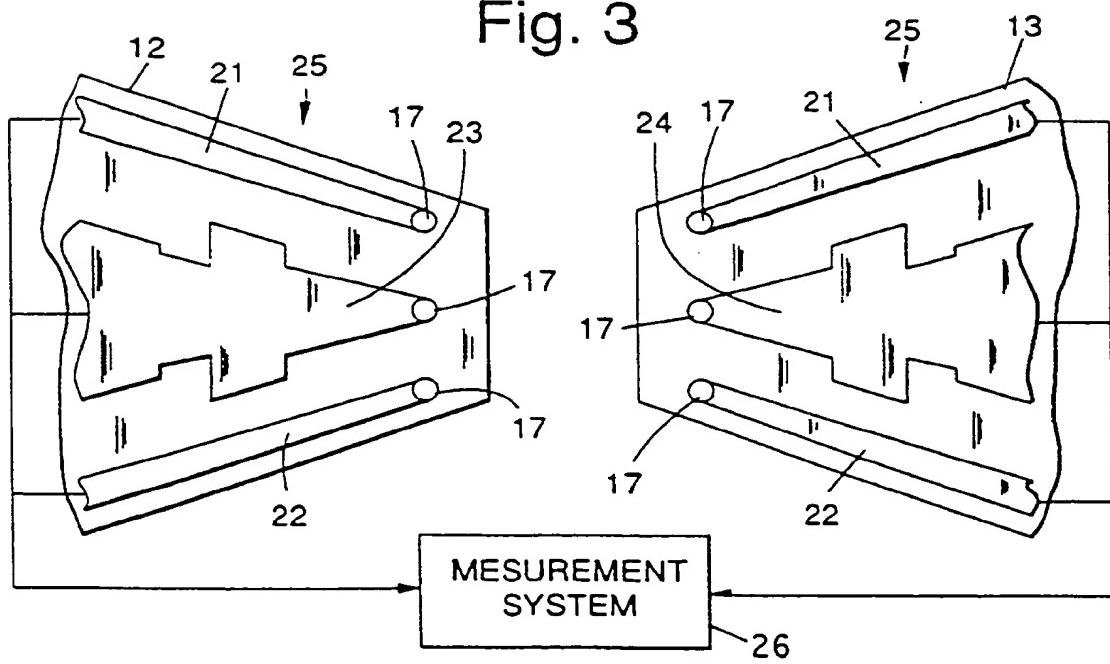
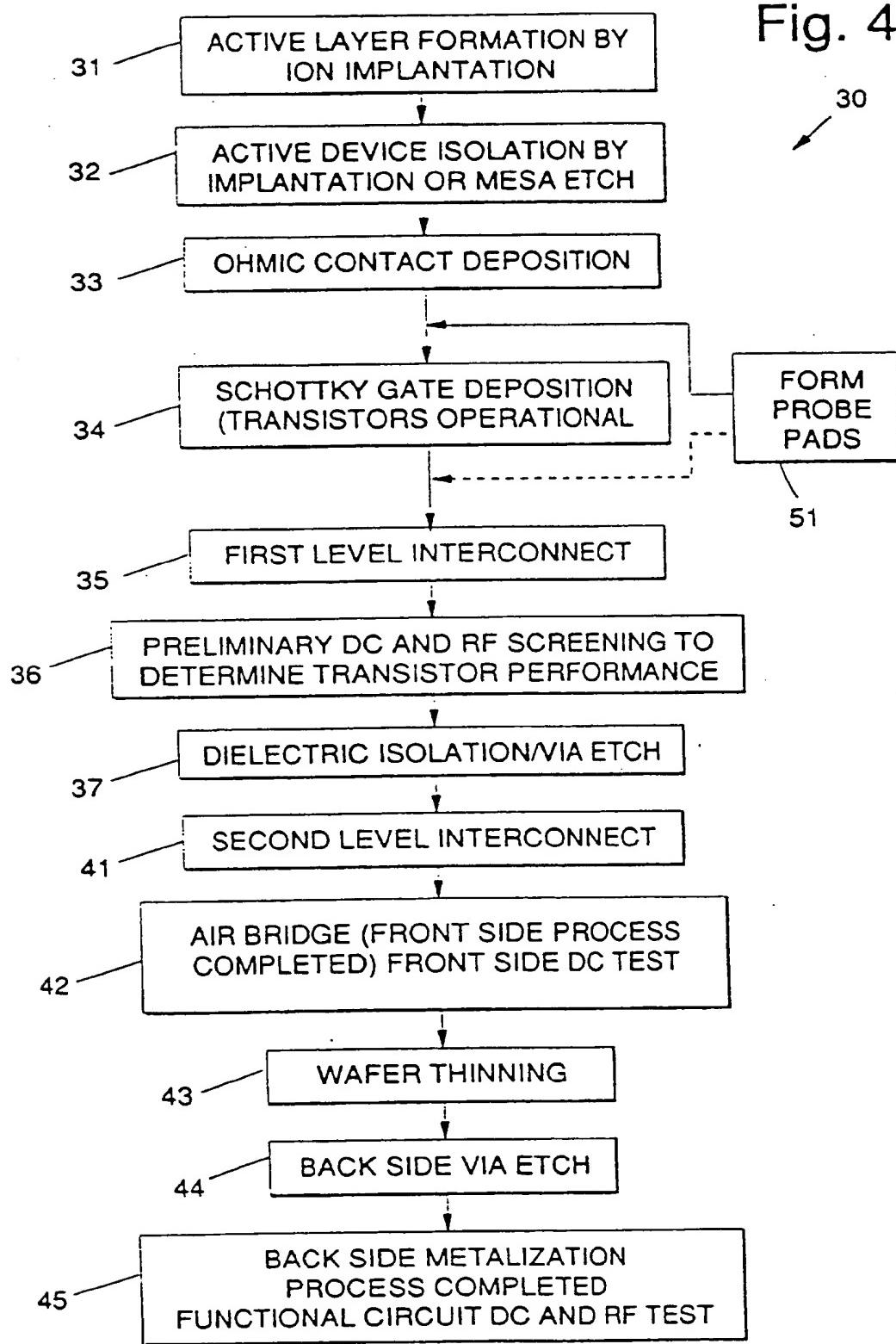


Fig. 4





European Patent
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EUROPEAN SEARCH REPORT

Application Number
EP 93 12 0025

DOCUMENTS CONSIDERED TO BE RELEVANT																											
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.CLS)																								
Y	ELECTRONICS. vol. 39, no. 21 , 17 October 1966 , NEW YORK US pages 94 - 98 J. KARDASH ET AL. 'A-c testing of wafer components sounds early circuit warning' * the whole document * ---	1-4,7,9, 11	H01L21/66 G01R1/067																								
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A	G-i-T, Fachz.Lab., 12.Jg., Heft 10, Okt.1968, pp. 1012-120 * the whole document * ---	1-10																									
A	DE-A-24 14 222 (FUJITSU LTD.) * the whole document * ---	1-10																									
A	US-A-4 853 624 (RABJOHN) * abstract; figures * ---	11																									
A	US-A-4 983 910 (MAJIDI-AHY ET AL.) * abstract; figures * -----	5,11																									
			TECHNICAL FIELDS SEARCHED (Int.CLS)																								
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<p>The present search report has been drawn up for all claims</p> <table border="1"> <tr> <td>Place of search</td> <td>Date of completion of the search</td> <td>Examiner</td> </tr> <tr> <td>THE HAGUE</td> <td>28 April 1994</td> <td>Prohaska, G</td> </tr> <tr> <td colspan="3">CATEGORY OF CITED DOCUMENTS</td> </tr> <tr> <td>X : particularly relevant if taken alone</td> <td colspan="2">T : theory or principle underlying the invention</td> </tr> <tr> <td>Y : particularly relevant if combined with another document of the same category</td> <td colspan="2">E : earlier patent document, but published on, or after the filing date</td> </tr> <tr> <td>A : technological background</td> <td colspan="2">D : document cited in the application</td> </tr> <tr> <td>O : non-written disclosure</td> <td colspan="2">L : document cited for other reasons</td> </tr> <tr> <td>P : intermediate document</td> <td colspan="2">& : member of the same patent family, corresponding document</td> </tr> </table>				Place of search	Date of completion of the search	Examiner	THE HAGUE	28 April 1994	Prohaska, G	CATEGORY OF CITED DOCUMENTS			X : particularly relevant if taken alone	T : theory or principle underlying the invention		Y : particularly relevant if combined with another document of the same category	E : earlier patent document, but published on, or after the filing date		A : technological background	D : document cited in the application		O : non-written disclosure	L : document cited for other reasons		P : intermediate document	& : member of the same patent family, corresponding document	
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